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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/023,170	02/13/1998	THOMAS J. HOLMAN	042390.P5346	6582
8791	7590	02/28/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			VERBRUGGE, KEVIN	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/023,170	HOLMAN, THOMAS J.
	<b>Examiner</b>	<b>Art Unit</b>
	Kevin Verbrugge	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 17 December 2004.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 21-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 21-40 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

## DETAILED ACTION

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/17/04 has been entered.

### ***Response to Amendment***

This non-final Office action is in response to the amendment filed 12/17/04 which amended claims 21 and 30. Claims 21-40 remain pending. All objections and rejections not repeated below are withdrawn.

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 21-40 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-31 of copending Application No. 09/023172 and claims 18-30 of copending Application No. 09/023234. Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences in the claims are immaterial.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 21 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner was not able to locate any passages in the specification which describe the newly claimed "plurality of memory

devices having different signal quality requirements from each other." Applicant is required to point out any and all supporting passages in the specification, if they exist.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Presumably the word --interface-- should be inserted between "direct" and "between" in line 6. That is how the claim has been interpreted for the purposes of this Office action. Applicant stated that this language was removed from the claim, however it remains so the rejection is repeated.

Claims 21 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "signal quality" in claims 21 and 30 is a relative term which renders the claim indefinite. The term "signal quality" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

It is not at all clear what is intended by the phrase "different signal quality requirements." How are the signal quality requirements of one memory device different than the signal quality requirements of another device? What are signal quality

requirements? There is no standard for ascertaining the degree of "signal quality" either in the claims or in the specification.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,319,591 to Takeda et al.

Regarding claims 21 and 30, Levy discloses memory modules with selectable byte addressing for a digital data processing system.

Levy shows the claimed memory bus as memory bus 40 in Fig. 1.

He shows the claimed system memory controller as memory management unit 22 and associative memory 24.

He shows the claimed memory module as memory module 30.

Levy shows the claimed first plurality of memory devices as low stacks 44 and high stacks 45 in Fig. 1.

He shows the claimed first memory module controller as memory transceiver 41 and memory control and timing circuit 42.

Levy's memory module controller (memory transceiver 41 and memory control and timing circuit 42) operates as claimed, serving as a direct interface between the memory devices and the system memory controller.

Levy does not explicitly disclose that his memory devices have different signal quality requirements. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use memory devices having different signal quality requirements since this would provide additional flexibility in the type of memory devices that could be used in Levy's memory modules.

Levy mentions using memory devices of different sizes at column 18, lines 28-55 (as mentioned by Applicant). He mentions using devices of "diverse characteristics" at column 2, lines 20-43, specifically mentioning magnetic core memory units and solid state or semiconductor random access memory units. He teaches that "Magnetic core memory units are very popular because they are reliable and retain data even in the absence of electrical power" and that "Semiconductor random access memory units are considerably faster than magnetic core memory units."

Furthermore, Levy specifically teaches using a combination of memory units in the same system. At column 2, lines 20-22, he teaches that "A memory arrangement for a data processing system thus may contain several types of memory units that have diverse characteristics." At column 3, lines 3-5, he discloses that a known "configuration includes both semiconductor random access memory units and magnetic core random access memory units".

And while it is true that he discloses differing types of memory units on a scale larger than a memory module (such as disk and drum devices and tape drives), he also teaches using differing types of memory units between memory modules and even within a single memory module. At column 18, lines 28-30, he teaches "the backup memory system 29 (Fig. 1) may comprise stacks having diverse characteristics." At column 24, lines 15-18 he teaches that "as shown especially in Fig. 11, each memory controller contains circuitry that enables diverse types of memory stacks to be intermixed within a given memory module." This is understood to mean that memory stacks within a single memory module in Levy's device can have different sizes (as long as the low stack and high stack of each pair have the same size, as taught at column 8, lines 27-28 and at column 16, lines 53-59) as well as different fundamental structures (for example, magnetic core vs. semiconductor, see the above passages as well as column 4, lines 35-37 and claim 5).

Takeda discloses a memory module with different kinds of memory devices and teaches that "It has thus been desired from the standpoint of memory module design to enable memory devices to be combined in a memory module without considering whether or not the memory devices are compatible in temperament" (column 1, lines 48-53) and that "it is an object of the present invention to consider how different kinds of memory devices in a memory module affect one another and to provide an improved memory module having a structure or an arrangement which can be manufactured without regard to the compatibility in temperament or characteristics between respective

memory devices" (column 1, lines 56-61). He goes on to discuss the different signal quality requirements of different types of memory devices at column 5, lines 11-45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include different types of memory devices having different signal quality requirements on Levy's memory modules because Levy shows intermixing memory modules having diverse characteristics and because Takeda teaches that it was desirable to do so when designing memory modules.

Regarding claims 22 and 31, Levy's memory control and timing circuit 42 includes the claimed clock generator since it generates a clock signal to drive the separate signals controlling the plurality of memory devices as claimed. Fig. 11 shows memory control and timing circuit 42 in detail, including control signal generator 145 (which outputs CLK MDR BYTE 0-3 signals), read timing generator 152, and write timing generator 156.

Regarding claims 23 and 32, Levy's memory module controller includes the claimed request handling logic in memory transceiver 41 and memory control and timing unit 42 since it examines a memory request to determine whether the memory request is addressed to the memory devices in its module and ignores the request if it is not addressed to its memory devices as claimed. More specifically, Fig. 11 shows memory control and timing unit 42 in more detail and Fig. 20 shows memory transceiver 41 in more detail. Fig. 11 includes the claimed request handling logic as the address

normalizing circuit 131A. If the memory is addressed to at least one of the memory devices on the module, then address normalizing circuit 131A permits the module to process the request. Otherwise, if the address request is not addressed to one of the memory devices on the module, then address normalizing circuit 131A prevents further processing by the module by asserting the address out of range signal shown being input to start memory cycle logic 150 (see column 16, lines 1-23).

Regarding claims 24 and 35, since Levy's memory module controller does not send signals to its memory devices when a memory request is not addressed to any of the devices, it can be said that the memory controller reduces the power to the memory devices (since power is transmitted on the signals, as discussed in the rejection of claim 33 above).

Regarding claims 25 and 37, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claims 26, 27, and 36, since Levy's memory module controller does not send signals to its memory devices when a memory request is not addressed to any

of the devices, it can be said that the memory controller decouples the memory devices from the memory bus.

Regarding claims 28, 29, and 34, Levy does not teach that his memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 33, Levy's memory module controller comprises the claimed power management unit because it controls power supplied to the memory devices as claimed. Levy's memory transceiver 41 and memory control and timing circuit 42 control all the signals and data supplied to the memory devices and thereby control the power supplied to the memory devices since power is transmitted on signals. In other words, power in the form of data, control, and timing signals is supplied to the memory devices. The broad language of the claim requires nothing more.

Regarding claim 39, Levy shows the claimed second memory module as memory module 31 in Fig. 1. Although he does not show its component parts, they are presumed analogous to those of memory module 30 precisely because they are not shown.

Regarding claim 38, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 40, Levy does not teach that his first and second plurality of memory devices (those in memory modules 30 and 31, respectively) have different signaling protocols, as claimed. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the different memory modules to use memory devices having different signaling protocols since the key system concern is interaction with the memory bus, not interaction with the memory devices. Additionally, systems were commonly configured with several memory module slots that were not all filled at original manufacture time allowing the user to add memory modules later to expand the system's capabilities, and while it is necessary that these added memory modules communicate as expected on the memory bus 40, the internal communications within the memory module are not specified by the system

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manufacturer and permit the use of different memory devices from one memory module to the next.

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Claims 24-29 and 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,319,591 to Takeda et al., further in view of U.S. Patent 5,257,233 to Schaefer.

Regarding claims 24, 26, 27, 33, 35, and 36, Levy does not explicitly teach that his memory module controller comprises a power management unit.

Schaefer discloses a low power memory module using restricted RAM activation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Schaefer's power reduction circuitry and techniques in Levy's memory modules to reduce the amount of power consumed. Schaefer teaches that unused memory devices may be powered down or placed in a reduced power mode to reduce the amount of power consumed by the module as a whole. By powering down certain memory devices, they are effectively decoupled from the memory bus.

Regarding claims 28, 29, and 34, neither Levy nor Schaefer teach that their memory devices and the memory bus operate at different voltages. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claims 25 and 37, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 38, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

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Claims 24-29 and 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,319,591 to Takeda et al., further in view of U.S. Patent 5,036,493 to Nielsen.

Regarding claims 24, 26, 27, 33, 35, and 36, Levy does not explicitly teach that his memory module controller comprises a power management unit.

Nielsen discloses a system and method for reducing power usage by multiple memory modules.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Nielsen's power reduction circuitry and techniques in Levy's memory modules to reduce the amount of power consumed. Nielsen teaches that unused memory devices may be powered down or placed in a reduced power mode to reduce the amount of power consumed by the module as a whole. By powering down certain memory devices, they are effectively decoupled from the memory bus.

Regarding claims 28, 29, and 34, neither Levy nor Nielsen teach that their memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed,

therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claims 25 and 37, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 38, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

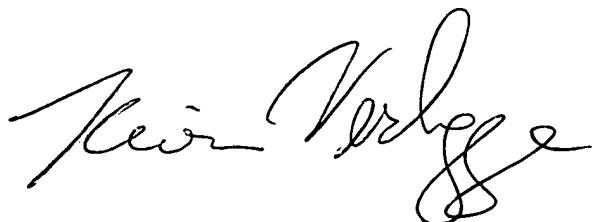
### ***Conclusion***

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (571) 272-4214.

Any response to this action should be labeled appropriately (including serial number, Art Unit 2188, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the Customer

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A handwritten signature in black ink, appearing to read "Kevin Verbrugge".

Kevin Verbrugge  
Primary Examiner  
Art Unit 2188